WHAT IS CLAIMED IS:

1. A semiconductor device comprising:

a first dielectric layer defining a copper containing feature; and

a thin stop layer formed on said first dielectric layer, said copper containing feature substantially free of damage resulting from forming an opening through said thin stop layer and a dielectric layer covering said thin stop layer.

2. The semiconductor device of claim 1 wherein said thin stop layer has a thickness less than 300Å.

3. The semiconductor device of claim 1, wherein said thin stop layer has a thickness of about 100Å.

4. The semiconductor device of claim 1 wherein damage to said copper containing feature is limited to a recess of less than about 150Å in the copper at the at via bottom.

5. The semiconductor device of claim 1 wherein said thin stop layer is multilayered.

6. The semiconductor device of claim 1 wherein said thin stop layer comprises an organic material.

7. The semiconductor device of claim 1 wherein said thin stop layer contains a metal.

8. The semiconductor device of claim 1 wherein said thin stop layer includes at least one of the materials selected from the group consisting of SiC, SiCN, SiCO, SiN, SiO, SiOCH, and combinations thereof.

9. A semiconductor device comprising an upper level of metallization covering a lower level of metallization which is substantially free of damage, said device comprising:

a substrate having a top surface, said top surface defining said lower level of metallization;

an etch stop layer having a thickness of less than 300Å deposited on top of said lower level of metallization;

a patterned layer of IMD (inter-metal dielectric) covering and in contact with said etch stop layer, said patterned layer of IMD defining a layout for said upper layer of metallization, said layout further including at least one area, where said layer of IMD and said etch stop layer are completely etched through said lower level of metallization substantially damage free; and

a metal layer filling said layout etched in said IMD layer forming said upper layer of metallization and in contact with said lower level of metallization.

10. The semiconductor device of claim 9 wherein said etch stop layer has a thickness of less than about 300Å.

11. The semiconductor device of claim 9 wherein said etch stop layer has thickness of about 100Å.

12. The semiconductor device of claim 9 wherein said etch stop layer is multilayered.

13. The semiconductor device of claim 9 wherein said etch stop layer includes an organic material.

14. The semiconductor device of claim 9 wherein said etch stop layer contains a metal.

15. The semiconductor device of claim 9 wherein said layer of etch stop layer comprises at least one of the materials selected from the group consisting of SiC, SiCN, SiCO, SiN, SiO and SiOCH.

16. The semiconductor device of claim 9 wherein said lower level of metallization comprises copper.

17. The semiconductor device of claim 9 wherein said metal layer filling said layout etched in said IMD layer comprises copper.

18. The semiconductor device of claim 9 wherein said substrate includes a dielectric layer and wherein said lower level of metallization is defined by a trench in said dielectric layer and further comprising a first metal seed layer on the bottom and side walls of said trench and a metal filling said trench.

19. The semiconductor device of claim 18 comprising a second metal seed layer between said first metal seed layer and said metal filling said trench.

20. The semiconductor device of claim 18 wherein said first metal seed layer is selected from the group consisting of copper, aluminum, gold, silver, tungsten and tantalum nitride.

21. The semiconductor device of claim 18 wherein at least one of said first and second metal seed layers are selected from the group consisting of copper, aluminum, gold, silver, tungsten and tantalum nitride.

22. The semiconductor device of claim 18 wherein said first and second metal seed layers are made from the same metal.

23. The semiconductor device of claim 17 wherein said metal filling said trench comprises copper.

24. A method for processing a semiconductor structure defining a metallization layer which results in said metallization layer being substantially free of damage comprising the steps of:

capping a top surface of said semiconductor structure that defines said metallization layer with a thin stop layer;

forming a layer of dielectric over said layer of thin stop, said layer of dielectric defining at least one area where said thin stop layer is exposed; and

removing said exposed thin stop layer to expose a top surface of said metallization layer which is substantially free of damage.

25. The method of claim 24 wherein said step of forming a layer of dielectric comprises forming a patterned layer of dielectric according to a patterned layer of resist, said patterned layer of dielectric defining a layout for an upper layer of metallization, and said step of removing further comprises removing said patterned layer of resist.

26. The method of claim 24 wherein said thin stop layer is deposited to a thickness of less than about 300Å.

27. The method of claim 24 wherein said thin stop layer is deposited to a thickness of about 100Å.

28. The method of claim 25 further comprising the step of filling said layout etched in said dielectric layer with a conductive metal, such as copper.

29. The method of claim 24 wherein said thin stop layer is an organic material.

30. The method of claim 24 wherein said thin stop layer contains a metal.

31. The method of claim 24 wherein said thin stop layer comprises at least one of the materials selected from the group consisting of SiC, SiCN, SiCO, SiN, SiO, SiOCH, and combinations thereof.

32. The method of claim 24 wherein said thin stop layer is multilayered.

33. The method of claim 24 wherein said thin stop layer is deposited by at least one of the processes selected from the group consisting of PVD (Plasma Vapor Deposition), CVD (Chemical Vapor Deposition), ALD (Atomic Layer Deposition), and Ion Beam Deposition.

34. The method of claim 24 wherein said thin stop layer is deposited at a temperature of between about 200°C and about 500°C.

35. The method of claim 24 further comprising the following steps for forming said semiconductor substrate:

depositing a dielectric layer;

forming a trench in said dielectric layer;

forming a metal seed layer over the dielectric layer with said trenches; and

depositing a metal in said trench.

36. The method of claim 35 further comprising forming a barrier layer over the surface of said trench prior to forming said seed layer.

37. The method of claim 36 wherein said barrier layer includes at least one of the materials selected from the group consisting of Ta, TaN, Ti, TiN, and combinations thereof.

38. The method of claim 37 wherein said step of forming a metal seed layer comprises the step of forming a first metal seed layer and then forming a second metal seed layer over said first seed layer.

39. The method of claim 38 wherein the surface of said second metal seed layer has a smooth surface.

40. The method of claim 37 wherein at least one of said first and second metal seed layers are selected from the group consisting of copper, aluminum, gold, silver, tungsten and tantalum nitride.

41. The method of claim 40 wherein said metal seed layers are deposited by a process selected from the group consisting of PVD (Plasma Vapor Deposition), CVD (Chemical Vapor Deposition), ALD (Atomic Layer Deposition), and ECP (Electro Chemical Process).

42. A method of forming the layout for an upper level of metallization in a semiconductor with reduced damage to a lower level of metallization comprising the steps of:

providing a substrate having a surface, said surface including a top surface of said lower level of metallization;

capping said lower level of metallization with a stop layer deposited to a thickness of less than 300Å over said surface;

forming a patterned layer of dielectric over said etch stop layer according to a patterned layer of resist on said dielectric layer, said patterned dielectric layer defining said layout for an upper level of metallization, and said layout including at least one area where said etch stop layer is exposed; and

removing said patterned resist and said exposed etch stop layer to expose, substantially damage free, a portion of said top surface of said lower level of metallization.

43. A method of forming an upper level of metallization in a semiconductor device with reduced damage to a lower level of metallization comprising the steps of:

providing a substrate having a top surface, said top surface defining said lower level of metallization;

capping said lower level of metallization with a stop layer deposited to a thickness of less than 300Å over said top surface;

depositing a layer of inter-metal dielectric (IMD) over said stop layer;

depositing and patterning a layer of resist to define a patterned mask over said layer of IMD;

etching said layer of IMD to remove material according to said mask, said removed material defining the layout for an upper level of metallization, and said layout including at least one area where said layer of IMD is completely etched through to expose said stop layer;

removing said patterned resist and said exposed stop layer; and

filling said layout etched in said IMD layer with metal to form said upper layer of metallization.